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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,991	05/02/2001	Jason Seung-Min Kim	NVID-P003124	5788

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EXAMINER	
MYERS, PAUL R	
ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
09/02/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/847,991	KIM ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *53-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *53-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/16/10 have been fully considered but they are not persuasive.

In regards to applicants argument that Zucker fails to teach or suggest said hardware semaphore unit: Zucker expressly teaches the processor sending a lock instruction to lock this memory. The bit in the hardware that receives this lock instruction and is set is a semaphore. While it is controller by software it has no choice but to be maintained in hardware. The examiner notes that Zucker's semaphore is set by software as opposed to being hardware controlled. It is still hardware instructed to be set by software. The examiner will however take the newly added word unit to mean that the semaphore is set by hardware as well as it being hardware. As such while Zucker teaches a hardware semaphore that is set be software. Zucker does not teach the newly added hardware semaphore unit that has hardware set the semaphore. The examiner notes previously cited reference Holt et al PN 5,394,551 that clearly teaches a hardware semaphore unit. The examiner also notes the previously cited reference to Tanenbaum that teaches hardware and software are logically equivalent.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 53 rejected under 35 U.S.C. 103(a) as being unpatentable over Zucker et al PN 3,805,247 in view of Frankeny et al PN 5,949,982 and Holt et al PN 5,394,551.

In regards to claims 53, 62, 71, 74: Zucker et al teaches a system (figure 8) comprising: a plurality of memory resources (subsets of memory modules attached to 76); a plurality of peripheral resources (Devices attached to 76); a plurality of processors (10); a memory controller (80, 84 and 86) coupled to said plurality of processors (10) and said plurality of memory resources (attached to 76), wherein said memory controller (80, 84 and 86) comprises a first resource controller (80) operable to control access of said plurality of processors (10) to said plurality of memory resources (attached to 76), wherein said first resource controller (80) is further operable to implement respective buses (connection from processors middle item 70 to the resource controllers OSN 84) for coupling said plurality of processors (10) to said plurality of memory resources (attached to 76), and wherein said memory controller (80, 84 and 86) is further operable to enable each processor (10) of said plurality of processors to simultaneously access (the communications are independent they are using different buses) a respective portion of a memory resource of said plurality of memory resources (attached to 76); and a peripheral controller (82, 84 and 86) coupled to said plurality of processors (10) and said plurality of peripheral resources (Devices attached to 76), wherein said peripheral controller (82, 84 and 86) comprises a second resource controller (82) operable to control access of said plurality of processors (10) to said plurality of peripheral resources (Devices attached to 76), and wherein said second resource controller (82) is further operable to implement respective buses (84 and 86 are crossbar switches) for coupling said plurality of processors (10) to said plurality of peripheral resources (Devices attached to 76). Zucker teaches preventing accessing to the same memory

modules at the same time implying accessing of different memories and different peripherals at the same time. (Column 11 line 28-43 and Column 10 line 41 to column 11 line 59). Zucker however does not expressly state that simultaneous access to different memories is performed. Frankeny expressly teaches simultaneous communications to different resources (Abstract, (Column 2 lines 7 to 23)). It would have been obvious to allow simultaneous communications to different resources in the system of Zucker because this would have prevented stalling a processor to access a resource that is not in use. Zucker teaches a semaphore that is set by a lock instruction as opposed to a semaphore unit that manages semaphores. Holt et al teaches a hardware semaphore unit that sets and maintains semaphores for accessing shared resources. It would have been obvious to have a hardware semaphore unit manage the semaphores because this would have removed the requirement of the processor having to manage the locking of the semaphore.

In regards to claims 54, 63: Zucker et al teaches a timer component (Clock 20 and 53) coupled to the controllers to control timing of the controllers.

In regards to claims 55-57, 64-66, 75-76: Zucker teaches the processors performing operations in parallel.

In regards to claims 58, 67, 73: Zucker teaches a semaphore (Lock Column 12 lines 18-32).

In regards to claims 59, 68: Zucker teaches the processors communicating through crossbar switches to memories and devices via cross bar switches. Zucker however does not expressly teach the processors being able to communicate with each other. Zucker does teach them both being able to access the lock to determine if the other processor is accessing the

desired shared resource. Frankeny et al teaches a plurality of processors communicating to each other and a plurality of memories and a plurality of I/O devices via a crossbar switch. It would have been obvious to allow the processors to also communicate with each other because this would have allowed for functions such as symmetrical multiprocessing.

In regards to claims 60, 69, 72: Zucker teaches the priority scheme being round robin (revolving priority Column 8 lines 11-21)

In regards to claims 61, 70: Zucker teaches the claimed computer system. Zucker however does not teach the system is portable. Official notice is taken that portable computers are well known. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include Zucker et al's design in a portable computer because this would have made it portable.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul R. Myers
Primary Examiner
Art Unit 2111

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